REMARKS

The above amendment is submitted in response to the outstanding Office Action in the immediate prior application, mailed October 4, 2000, for consideration in the present continued prosecution application. This amendment is identical to that discussed with Examiner Collins on April 27, 2001, and the undersigned attorney and applicants greatly appreciate the Examiner's time and courtesy shown them. Subject to an updated search, we understand that the above amendments overcome the outstanding rejections, which are briefly addressed below in accordance with those discussions. Applicants also submit herewith a Supplemental Information Disclosure Statement for the Examiner's receipt and consideration.

Rejection Based on Teong:

Claims 1, 6, 11, 18, 24 and 30 stood rejected in the immediate prior application based on U.S. Patent No. 5,693,563 to Teong. As noted to the Examiner, Teong fails to disclose an electrochemical metal deposition process. Rather, Teong discloses a process for applying a silicone oxide insulating layer, then a barrier layer, than an insulating layer, and then a copper layer "by vacuum evaporation or CVD", then followed by chemical mechanical planarization, and then deposition of another barrier layer followed by a passivation layer. In contrast to the Teong reference, the present invention calls for depositing copper using an electrochemical process. Further, Teong fails to disclose the process including elevated temperature annealing.

Rejection Based on Teong and Chan:

Claims 2-5, 7-10, 12-17, 19-23, 25-29 and 31 also stand rejected under 35 U.S.C. § 103 based on the combination of Teong with U.S. Patent No. 6,100,195 to Chan et al. Initially applicants respectfully note that Chan is not directed to the annealing of copper to increase grain size, rather it is directed toward processing for alloying copper with aluminum, platinum or palladium. Moreover, applicants note that Chan et al. has an effective 102(e) date of

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December 28, 1998, the date on which that application was filed. Applicants respectfully note that the above application was filed on February 4, 1998, and thus Chan is not prior art to the above application.

Summary

In view of the above, applicants respectfully request reconsideration and passage of all claims pending inclusive of Claims 1, 3, 4, 6, 8-17 and 24-31 to issue. Should there be any remaining questions, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to the Commissioner for Patents, Washington, D.C. 20231, on the below date.

Date: June 13, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE JUNE 13, 2001

In the Claims:

Claims 2, 5, 7 and 18-23 have been canceled.

1. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper [metallization]metal comprising[the steps of]:

depositing [a]copper [layer]into the recessed micro-structures [with]using [a]an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the [deposited]surface of the semiconductor workpiece with the deposited copper to an elevated temperature annealing process at a temperature below about 100 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper.

3. (Amended) A method as claimed in Claim 1 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

4. (Amended) A method as claimed in Claim 1 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

6. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with [metallization]copper metal comprising[the steps of]:

depositing[a metal layer] copper into the recessed microstructures[with a] using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the [deposited metal]surface of the semiconductor workpiece and the deposited copper to an elevated temperature annealing process at a temperature at or below about

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[100]250 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper.

8. (Amended) A method as claimed in Claim 6 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small metal grain size.

9. (Amended) A method as claimed in Claim 6 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small metal grain size.

10. (Amended) A method [as claimed in claim 6 wherein the annealing process is carried out at ambient room temperature]for filling recessed microstructures at a surface of a semiconductor workpiece, the workpiece including at least one low-K dielectric layer, with copper metal comprising:

depositing copper into the recessed micro-structures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece with the deposited copper to an elevated temperature annealing process at a temperature selected to be below a predetermined temperature at which the low-K dielectric layer would suffer substantial degradation.

11. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper [metallization]metal comprising [the steps of]:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

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preparing a surface of the workpiece including the recessed microstructures with a metal seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

[allowing]annealing the electrochemically deposited copper layer [to self-anneal]at an elevated temperature selected to be below a predetermined temperature at which time the low-K dielectric layer would substantially degrade for a predetermined period of time[at ambient room temperature]; and

removing copper metallization from the surface of the workpiece except from the recessed microstructures, [said removing step occurring]after the [predetermined period of time has elapsed]annealing of the copper.

13. (Amended) A method as claimed in Claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a metal seed layer over the barrier layer.

16. (Amended) A method as claimed in Claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a metal seed layer over the adhesion layer.

24. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper [metallization]metal comprising[the steps of]:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

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applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process generating copper grains that are sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrochemically deposited copper layer to an annealing process at a temperature at or below about [100]250 to 300 degrees Celsius to increase the copper grain size.

30. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper [metallization]metal comprising[the steps of]:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a [seed]barrier layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece using a process that generates copper grains having a size sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.

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